Technical Information

ARM-related

JTAG / SWD / SWV / ETM Target Interfaces

Sep. 18, 2015
Fourth Edition

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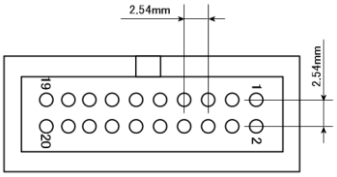
Document change history

First Edition	Sep. 11, 2009	Initial edition
Second Edition	Nov. 13, 2009	・Added the descriptions on CPU core "ARM" and "PALMiCE3 ARM (JTAG200)" to Technical Information reference chart and Product purchase chart. ・Corrected the Product purchase chart. Technical Information ④ and ⑥ correspond to PALMiCE3 CM3 (ETM200) only. However, PALMiCE3 CM3(ETM200) is a product to be released in the future. ・Added the note on $\overline{\text{SRST}}$ signal in respective signal tables. "$\overline{\text{SRST}}$ signal is an open-collector output."
Third Edition	Mar. 04, 2011	・PALMiCE3 CM3(ETM200) has already been released (Dec. 2009). Deleted the following description: "To be released in the future." ・"Supported connectors" Added graphic images of the connectors. ・"Product purchase chart" Added graphic images of the optional products. ・Added the note on $\overline{\text{SRST}}$ signal in respective signal tables. ・Changed the note on $\overline{\text{TRST}}$ signal in respective signal tables. ・Deleted CPU core options from Technical Information reference chart and Product purchase chart. For supported CPUs, refer to Product Summary of respective products up on our website. ・Deleted the description of the case where ETM is not used and half-pitch (1.27mm) connector is used. When you use them, please contact us.
Fourth Edition	Sep. 18, 2015	・Added an item to Applicable products: PALMiCE2H ARM (ETM383) ・Following addition of an item to Applicable products mentioned above, added the description on PALMiCE2H to Technical Information reference chart and Product purchase chart. ・Following addition of an item to Applicable products mentioned above, added ⑦⑧⑨⑩ to pages on target interface details. ・Placed specifications of the target interface on the debugger side. PALMiCE3 PALMiCE3 JTAG200 model Hardware Manual) PALMiCE2H Extracted from PALMiCE2H ARM User's Manual) ・Supported connectors – 38-pin Mictor connector Changed the recommended connectors. [Before change] 2-767004-2 / 767054-1 / 767061 (* RoHS-non-compliant products) [After change] 2-5767004-2 / 5767054-1 / 5767061-1 (*RoHS-compliant products) ・Supported connectors Added the note. ・Product purchase chart Added "PALMiCE3-ARM (JTAG200)" to ⑦ to ⑩. ・Added notes on the $\overline{\text{TRST}}$ signal described in ② (Using 20-pin 2.54 mm-pitch connector + JTAG interface). ・Added ⑥ (Using 20-pin 1.27 mm-pitch connector + JTAG interface). ・According to the above addition, incremented the heading number ⑥ and subsequent numbers by one. ・In accordance with J-STICK sales termination, deleted J-STICK descriptions from the applicable products and the product purchase chart.

Supported connectors

(For detailed dimensions of the connectors, refer to the documentations by respective manufacturers of the connectors.)

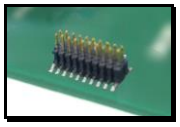
20-pin 2.54mm-pitch connector

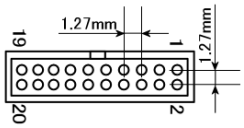


(Top view on the target board)

Recommended connector
Manufacturer: OMRON Corporation
Model : XG4C-2031

20-pin 1.27mm-pitch connector

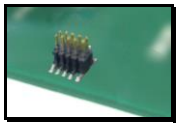


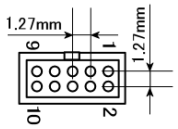


(Top view on the target board)

Recommended connector
Manufacturer: Samtec, Inc.
Model : FTSH-110-01-L-DV-K

10-pin 1.27mm-pitch connector

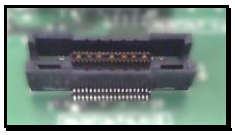


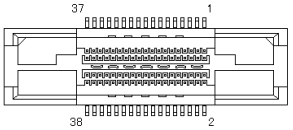


(Top view on the target board)

Recommended connector
Manufacturer: Samtec, Inc.
Model : FTSH-105-01-L-DV-K

38-pin Mictor connector





(Top view on the target board)

Recommended connector
Manufacturer: AMP
Model : Mictor connector
2-5767004-2 / 5767054-1 / 5767061-1

*** Please look at the pin configuration diagram and make sure that the connector is in the right direction before connecting.**
Moreover, please check the pin number in the corresponding signal table and make sure the signal and the pin numbers match.

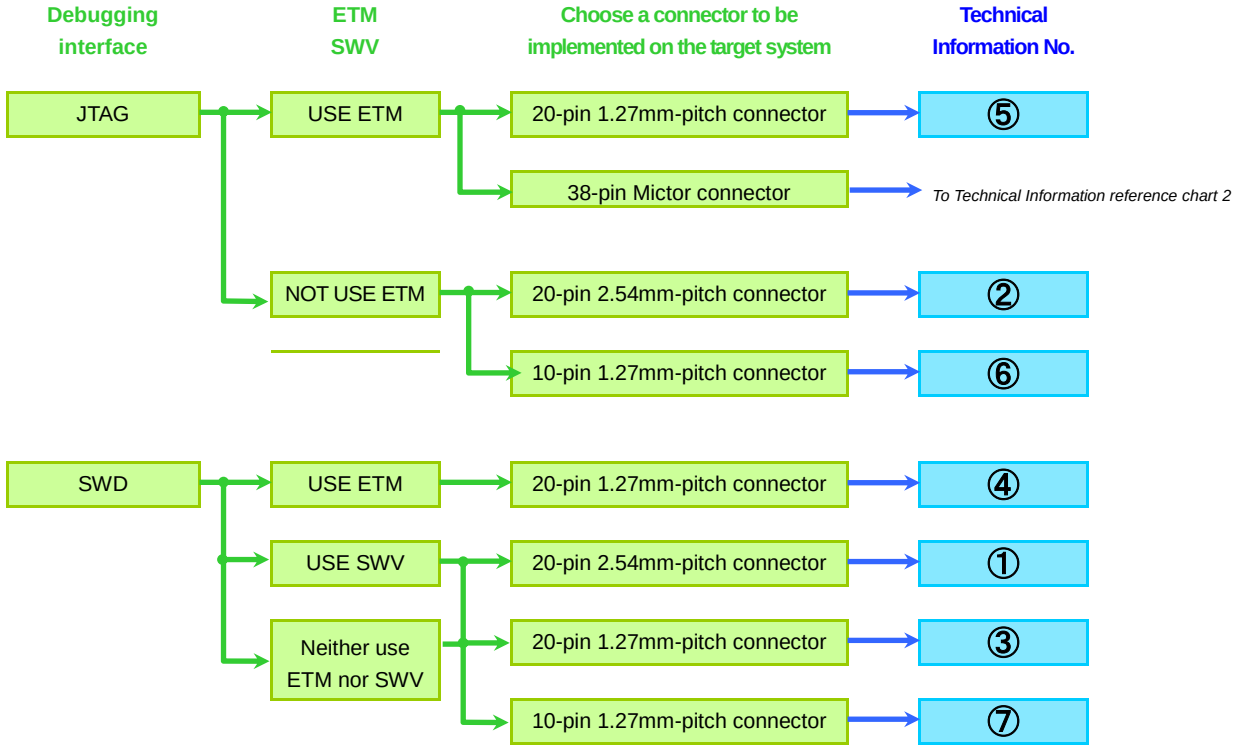
Applicable products

This manual is applicable for the following products.

- PALMiCE3 ARM (JTAG200)
- PALMiCE3 CM3 (ETM200)
- PALMiCE2H ARM (ETM383)

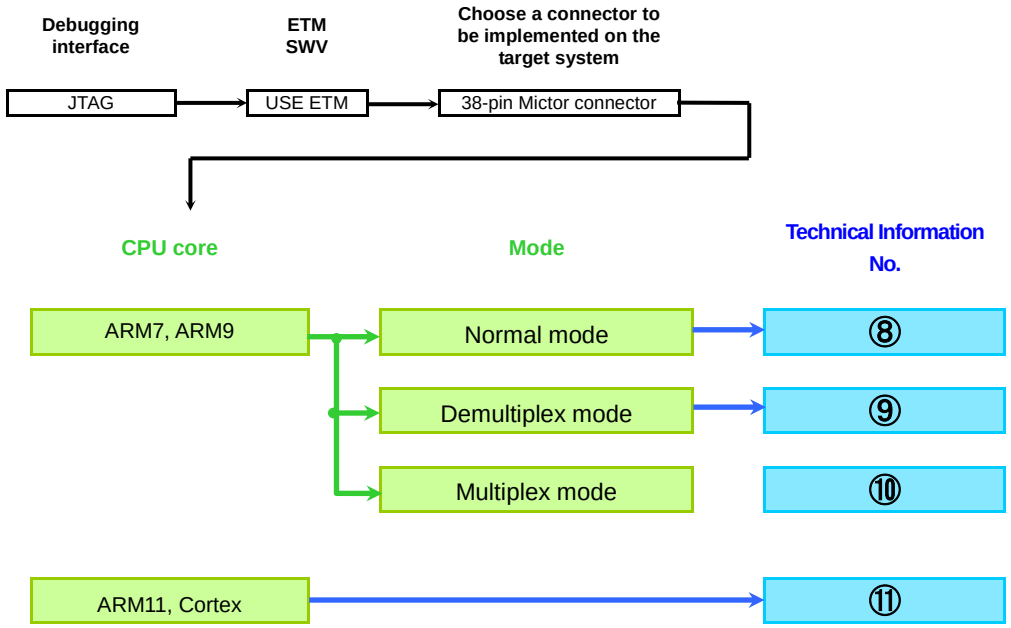
Technical Information reference chart 1

Depending on the target interface you use, Technical Information you should refer to will be different.
Based on the chart below, consult the applicable Technical Information.



* : Only those combinations available for selection are given. For other combinations, please contact us.

Technical Information reference chart 2



* : Only those combinations available for selection are given.

Product purchase chart

Depending on the target interface you use, the composition of product and optional product you should purchase will differ.
Based on the Technical Information No. (See "Technical Information reference chart" on the previous page), choose the product.

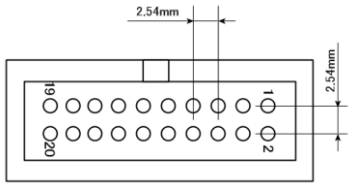
* : Only those products available for selection are given.

Technical Information No.	Product name *1		Required optional product
①	PALMiCE3 ARM (JTAG200) PALMiCE3 CM3 (ETM200)	+	ADP-SWJ-HP20-MIL20
②	PALMiCE3 ARM (JTAG200) PALMiCE3 CM3 (ETM200) PALMiCE2H ARM (ETM383)	+ +	ADP-SWJ-HP20-MIL20 ADP-ETM-JTAG20
③	PALMiCE3 ARM (JTAG200) PALMiCE3 CM3 (ETM200) PALMiCE2H ARM (ETM383)	+	SWJ-PRB-MIL20-20HP
④ ⑤	PALMiCE3 CM3 (ETM200) PALMiCE2H ARM (ETM383)		
⑥	PALMiCE3 ARM (JTAG200)	+	SWJ-PRB-MIL20-20HP
⑦	PALMiCE3 ARM (JTAG200)	+	SWJ-PRB-MIL20-10HP
⑧ ⑨ ⑩	PALMiCE2H ARM (ETM383) PALMiCE3 ARM (JTAG200)	+ +	ADP-JTAG20-ETM
⑪	PALMiCE2H ARM (ETM383) PALMiCE3 ARM (JTAG200)	+ +	ADP-JTAG20-ETM

*1 : For the CPUs supported by respective products, refer to Product Summary of respective products up on Computex website.

20-pin 2.54mm-pitch connector

Target connector specifications



(Top view on the target board)

Recommended connector

Manufacturer: OMRON Corporation

Model: XG4C-2031

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

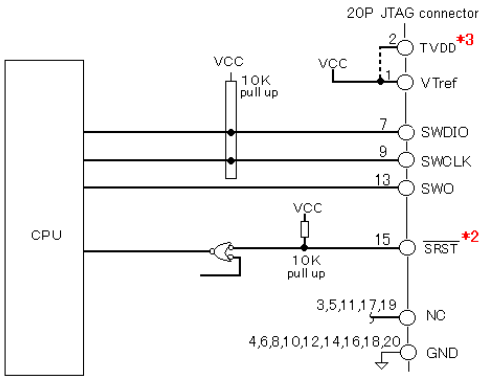
① SWD interface

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	VTref	Output	2	TVDD*3	Output
3	NC		4	GND	
5	NC		6	GND	
7	SWDIO	Input/Output	8	GND	
9	SWCLK	Input	10	GND	
11	NC		12	GND	
13	SWO	Output	14	GND	
15	$\overline{\text{SRST}}$*2		16	GND	
17	NC		18	GND	
19	NC		20	GND	

*1: Input/output is based on the target system.
*2: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*3: The signal is not used by Computex-made debugger; it can be left unconnected.

Target connection reference diagram



- This interface does not use $\overline{\text{TRST}}$.
  If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

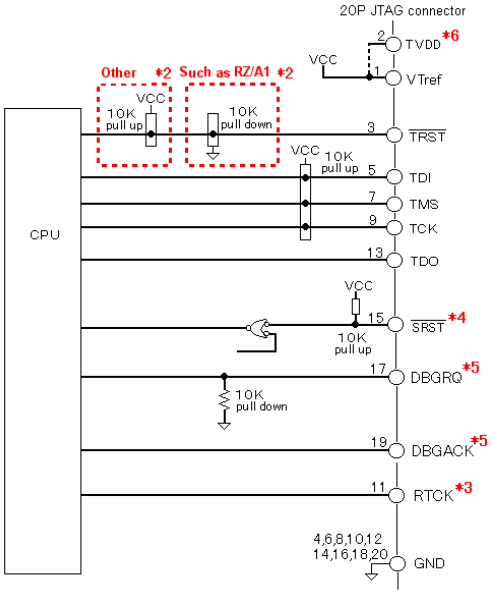
② JTAG interface

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	VTref	Output	2	TVDD*6	Output
3	$\overline{\text{TRST}}$*2	Input	4	GND	
5	TDI	Input	6	GND	
7	TMS	Input	8	GND	
9	TCK	Input	10	GND	
11	RTCK*3	Output	12	GND	
13	TDO	Output	14	GND	
15	$\overline{\text{SRST}}$*4	Input	16	GND	
17	DBGRQ*5	Input	18	GND	
19	DBGACK*5	Output	20	GND	

*1: Input/output is based on the target system.
*2: For some CPUs (such as Renesas Electronics RZ/A1L), pull-down may be required. Check the data sheet of the CPU to be used, and use either pull-up or pull-down.
*3: If the CPU does not present the pin or if you do not use RTCK, leave it as N.C..
*4: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*5: In the CPUs that do not present this signal, leave the pin unconnected in open state.
*6: The signal is not used by Computex-made debugger; it can be left unconnected.

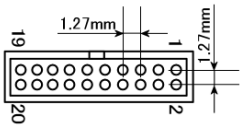
Target connection reference diagram



- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

20-pin 1.27mm-pitch connector

Target connector specifications



(Top view on the target board)

Recommended connector

Manufacturer: Samtec, Inc.

Model: FTSH-110-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

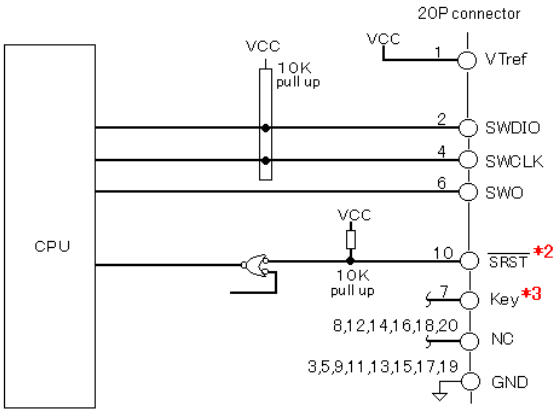
③ SWD interface

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	Vtref	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO	Output
7	Key*3		8	NC	
9	GND		10	$\overline{\text{SRST}}$*2	Input
11	GND		12	NC	
13	GND		14	NC	
15	GND		16	NC	
17	GND		18	NC	
19	GND		20	NC	

*1: Input/output is based on the target system.
*2: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*3: "Key" is intended for protection against wrong insertion.

Target connection reference diagram



- This interface does not use $\overline{\text{TRST}}$.
  If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

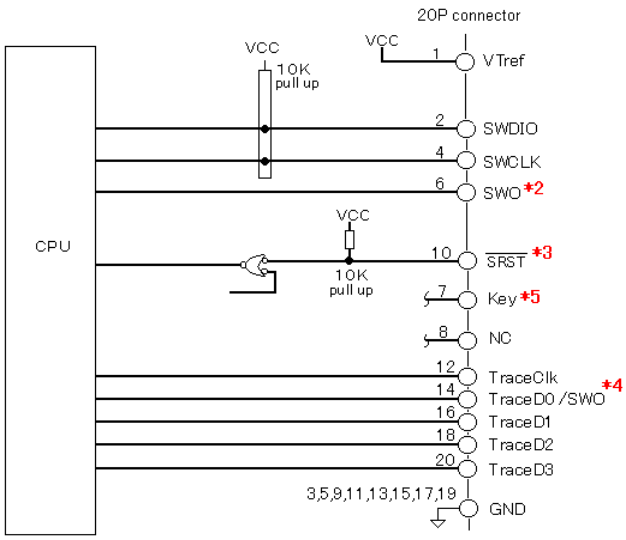
④ SWD interface + Trace

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	Vtref	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO*2	Output
7	Key*5		8	NC	Input
9	GND		10	$\overline{\text{SRST}}$*3	Input
11	GND		12	TraceClk	Output
13	GND		14	TraceD0/SWO*4	Output
15	GND		16	TraceD1	Output
17	GND		18	TraceD2	Output
19	GND		20	TraceD3	Output

*1: Input/output is based on the target system.
*2: Connect the signal dedicated to SWO. The pin can be left N.C. if you are using Pin No. 14 as SWO (See *4).
*3: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*4: In some CPUs, SWO and TraceD0 are multiplexed.
In the case of such pin, connect SWO signal not to Pin No. 6 but to Pin No.14 even when you intend to use Pin No. 14 as SWO, not as TraceD0.
*5: "Key" is intended for protection against wrong insertion.

Target connection reference diagram



- This interface does not use $\overline{\text{TRST}}$.
  If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

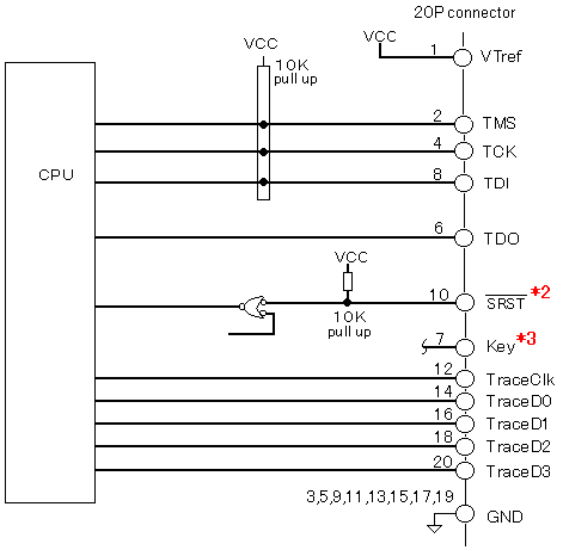
⑤ JTAG interface + Trace

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	Vtref	Output	2	TMS	Input/Output
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key*3		8	TDI	Input
9	GND		10	$\overline{\text{SRST}}$*2	Input
11	GND		12	TraceClk	Output
13	GND		14	TraceD0	Output
15	GND		16	TraceD1	Output
17	GND		18	TraceD2	Output
19	GND		20	TraceD3	Output

*1: Input/output is based on the target system.
*2: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*3: "Key" is intended for protection against wrong insertion.

Target connection reference diagram



- This interface does not use $\overline{\text{TRST}}$.
  If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

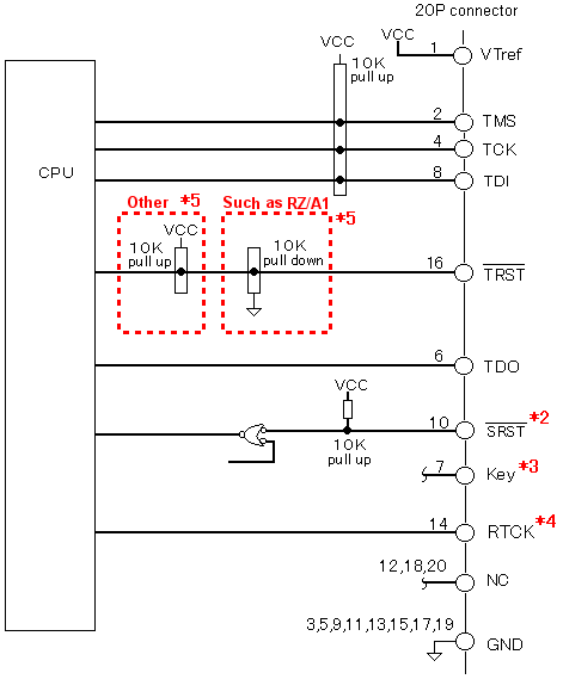
⑥ JTAG interface

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	Vtref	Output	2	TMS	Input/Output
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key*3		8	TDI	Input
9	GND		10	$\overline{\text{SRST}}$*2	Input
11	GND		12	NC	
13	GND		14	RTCK*4	Output
15	GND		16	$\overline{\text{TRST}}$*5	Input
17	GND		18	NC	
19	GND		20	NC	

*1: Input/output is based on the target system.
*2: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*3: "Key" is intended for protection against wrong insertion.
*4: If the CPU does not present the pin or if you do not use RTCK, leave it as N.C..
*5: For some CPUs (such as Renesas Electronics RZ/A1L), pull-down may be required. Check the data sheet of the CPU to be used, and use either pull-up or pull-down.

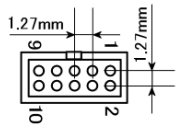
Target connection reference diagram



- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

10-pin 1.27mm-pitch connector

Target connector specifications



(Top view on the target board)

Recommended connector

Manufacturer: Samtec, Inc.

Model: FTSH-105-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

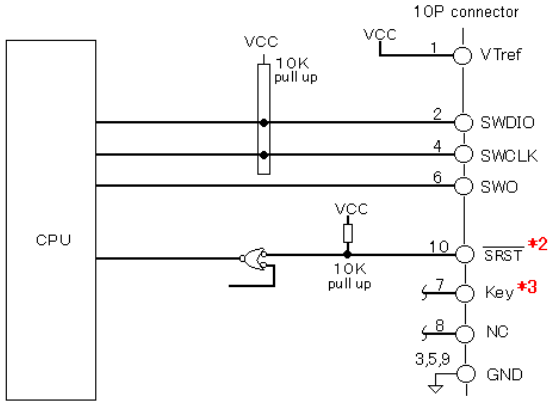
⑦ SWD interface

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	VTref	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO	Output
7	Key*3		8	NC	Input
9	GND		10	$\overline{\text{SRST}}$*2	Input

*1: Input/output is based on the target system.
*2: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*3: "Key" is intended for protection against wrong insertion.

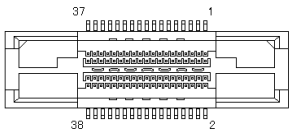
Target connection reference diagram



- This interface does not use $\overline{\text{TRST}}$.
  If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

38-pin Mictor connector

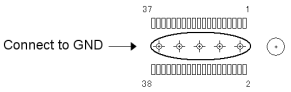
Target connector specifications



(Top view on the target board)

Recommended connector
Manufacturer :AMP
Model : Mictor connector
2-767004-2 / 767054-1 / 767061

In mounting ETM connector, place it to the position as close as possible to CPU so that wiring pattern length will be minimized. Also in mounting JTAG connector, place it to the position close to ETM connector.
In addition, you will need to connect the Grand Bus Leads of ETM connector to the GND.



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

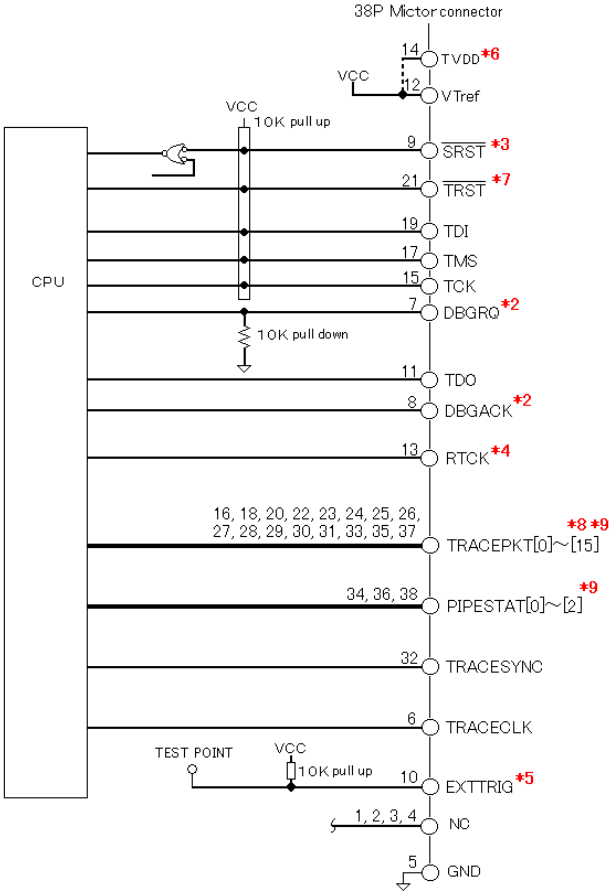
⑧ JTAG interface + ETM - Normal mode

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	TRACECLK	Output
7	DBGRQ*2	Input	8	DBGACK*2	Output
9	$\overline{\text{SRST}}$*3	Input	10	EXTTRIG*5	Input
11	TDO	Output	12	VTref	Output
13	RTCK*4	Output	14	TVDD*6	Output
15	TCK	Input	16	TRACEPKT7*8	Output
17	TMS	Input	18	TRACEPKT6*8	Output
19	TDI	Input	20	TRACEPKT5*8	Output
21	$\overline{\text{TRST}}$*7	Input	22	TRACEPKT4*8	Output
23	TRACEPKT15*8	Output	24	TRACEPKT3	Output
25	TRACEPKT14*8	Output	26	TRACEPKT2	Output
27	TRACEPKT13*8	Output	28	TRACEPKT1	Output
29	TRACEPKT12*8	Output	30	TRACEPKT0	Output
31	TRACEPKT11*8	Output	32	TRACESYNC	Output
33	TRACEPKT10*8	Output	34	PIPESTAT2	Output
35	TRACEPKT9*8	Output	36	PIPESTAT1	Output
37	TRACEPKT8*8	Output	38	PIPESTAT0	Output

*1: Input/output is based on the target system.
*2: In the CPUs that do not present this signal, leave the pin unconnected in open state.
*3: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*4: If the CPU does not present the pin or if you do not use RTCK, leave it as N.C..
*5: The signal is not used by Computex-made debugger.
*6: The signal is not used by Computex-made debugger; it can be left unconnected.
*7: If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
*8: If the trace data is of 4-bit, connect signals TRACEPKT4 - 15, or if of 8-bit, connect signals TRACEPKT8 - 15, to GND.
*9: For the names of signals corresponding to respective pin No., see the table of Signals.

Target connection reference diagram



■ Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

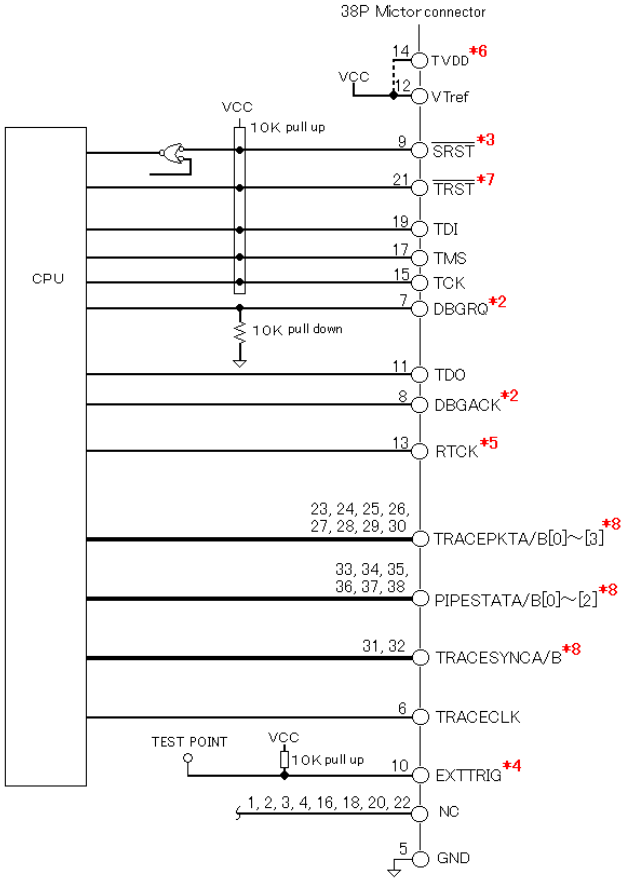
⑨ JTAG interface + ETM – Demultiplex mode

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	TRACECLK	Output
7	DBGRQ *2	Input	8	DBGACK *2	Output
9	$\overline{\text{SRST}}$*3	Input	10	EXTTRIG *4	Input
11	TDO	Output	12	VTref	Output
13	RTCK *5	Output	14	TVDD *6	Output
15	TCK	Input	16	NC	
17	TMS	Input	18	NC	
19	TDI	Input	20	NC	
21	$\overline{\text{TRST}}$ *7	Input	22	NC	
23	TRACEPKTB3	Output	24	TRACEPKTA3	Output
25	TRACEPKTB2	Output	26	TRACEPKTA2	Output
27	TRACEPKTB1	Output	28	TRACEPKTA1	Output
29	TRACEPKTB0	Output	30	TRACEPKTA0	Output
31	TRACESYNCB	Output	32	TRACESYNCA	Output
33	PIPESTATB2	Output	34	PIPESTATA2	Output
35	PIPESTATB1	Output	36	PIPESTATA1	Output
37	PIPESTATB0	Output	38	PIPESTATA0	Output

*1: Input/output is based on the target system.
*2: In the CPUs that do not present this signal, leave the pin unconnected in open state.
*3: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*4: The signal is not used by Computex-made debugger.
*5: f the CPU does not present the pin or if you do not use RTCK, leave it as N.C..
*6: The signal is not used by Computex-made debugger; it can be left unconnected.
*7: If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
*8: For the names of signals corresponding to respective pin No., see the table of Signals.

Target connection reference diagram



■ Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

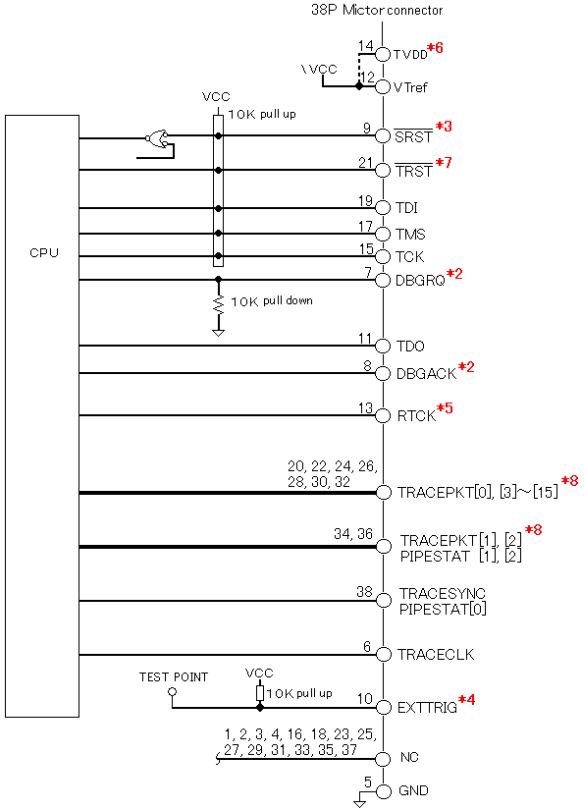
⑩ JTAG interface + ETM – Multiplex mode

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	TRACECLK	Output
7	DBGRQ*2	Input	8	DBGACK*2	Output
9	$\overline{\text{SRST}}$*3	Input	10	EXTTRIG*4	Input
11	TDO	Output	12	VTref	Output
13	RTCK*5	Output	14	TVDD*6	Output
15	TCK	Input	16	NC	
17	TMS	Input	18	NC	
19	TDI	Input	20	TRACEPKT[14,15]	Output
21	$\overline{\text{TRST}}$*7	Input	22	TRACEPKT[12,13]	Output
23	NC		24	TRACEPKT[10,11]	Output
25	NC		26	TRACEPKT[8,9]	Output
27	NC		28	TRACEPKT[6,7]	Output
29	NC		30	TRACEPKT[4,5]	Output
31	NC		32	TRACEPKT[0,3]	Output
33	NC		34	PIPESTAT2+TRACEPKT2	Output
35	NC		36	PIPESTAT1+TRACEPKT1	Output
37	NC		38	PIPESTAT0+TRACESYNC	Output

*1: Input/output is based on the target system.
*2: In the CPUs that do not present this signal, leave the pin unconnected in open state.
*3: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*4: The signal is not used by Computex-made debugger.
*5: f the CPU does not present the pin or if you do not use RTCK, leave it as N.C..
*6: The signal is not used by Computex-made debugger; it can be left unconnected.
*7: If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
*8: For the names of signals corresponding to respective pin No., see the table of Signals.

Target connection reference diagram



■ Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

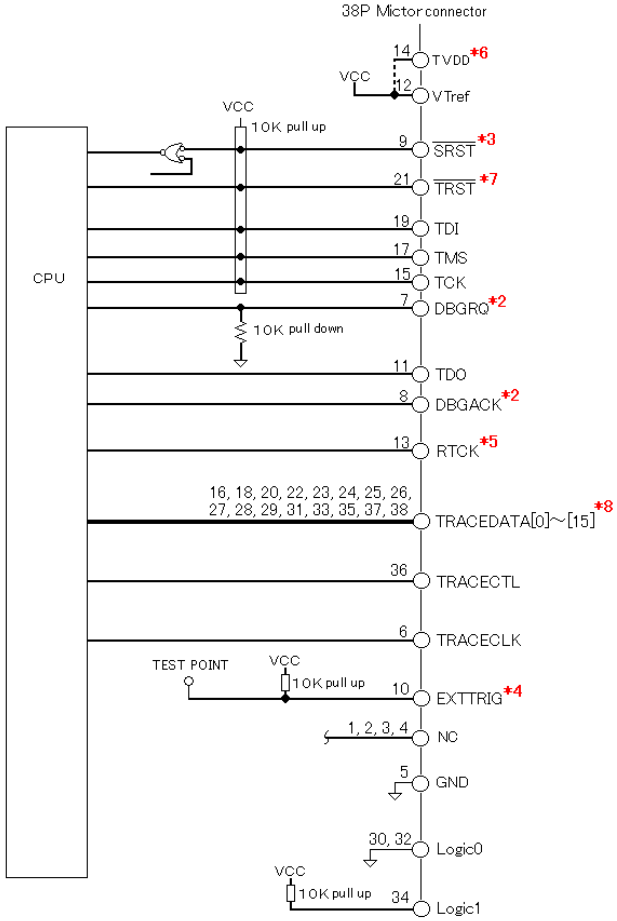
⑪ JTAG interface + ETM / PTM

Signals

Pin No.	Signal	Input/ Output*1	Pin No.	Signal	Input/ Output*1
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	TRACECLK	Output
7	DBGRQ*2	Input	8	DBGACK*2	Output
9	$\overline{\text{SRST}}$*3	Input	10	EXTTRIG*4	Input
11	TDO	Output	12	VTref	Output
13	RTCK*5	Output	14	TVDD*6	Output
15	TCK	Input	16	TRACEDATA[7]	Output
17	TMS	Input	18	TRACEDATA[6]	Output
19	TDI	Input	20	TRACEDATA[5]	Output
21	$\overline{\text{TRST}}$*7	Input	22	TRACEDATA[4]	Output
23	TRACEDATA[15]	Output	24	TRACEDATA[3]	Output
25	TRACEDATA[14]	Output	26	TRACEDATA[2]	Output
27	TRACEDATA[13]	Output	28	TRACEDATA[1]	Output
29	TRACEDATA[12]	Output	30	Logic0	Output
31	TRACEDATA[11]	Output	32	Logic0	Output
33	TRACEDATA[10]	Output	34	Logic1	Output
35	TRACEDATA[9]	Output	36	TRACECTL	Output
37	TRACEDATA[8]	Output	38	TRACEDATA[0]	Output

*1: Input/output is based on the target system.
*2: In the CPUs that do not present this signal, leave the pin unconnected in open state.
*3: $\overline{\text{SRST}}$ signal is an open-collector output.
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
*4: The signal is not used by Computex-made debugger.
*5: If the CPU does not present the pin or if you do not use RTCK, leave it as N.C..
*6: The signal is not used by Computex-made debugger; it can be left unconnected.
*7: If the target CPU presents a pin specifically for $\overline{\text{TRST}}$, pull it up with 10K ohmic value.
*8: For the names of signals corresponding to respective pin No., see the table of Signals.

Target connection reference diagram



■ Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

PALMiCE3 JTAG200 model

Hardware Manual

(Fifth Edition)

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Chapter 1 Getting Started

1.1 Introduction

PALMiCE3 JTAG200 model is an on-chip debugger that supports ARM-made core CPUs.

Its main features are as follows:

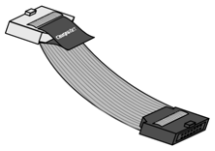
- Provides multi-core support
- No power supply to PALMiCE3 is required (with VBus support)
- Allows downloading to external flash memory and its debugging
- Supports on-chip flash memory
- Versatile
- Supports USB Standard Revision2.0 high-speed and full-speed
- Allows downloading of the latest CSIDE from the Internet
- Designed with palm-sized, light, and compact body

1.2 Product Composition Contents

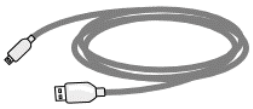
Product composition of PALMiCE3 JTAG200 model is as follows.

- PALMiCE3 JTAG200 model ····· x 1

- Target cable (Specifically for PALMiCE3) ····· x 1



- USB cable ····· x 1



- Product name sticker ····· x 1

- Software (CD-ROM) *1 ····· x 1

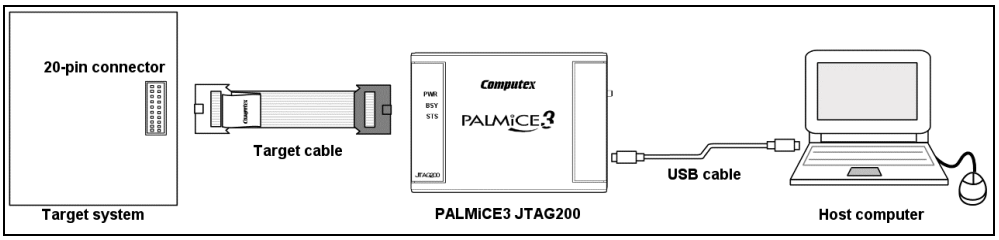
***1 : Its name varies depending on CSIDE, the debugger software you purchased.**

1.3 Connection structure

PALMiCE3 is to be connected to the host computer with the USB cable included with the product. PALMiCE3 is to be connected to the target system with the target cable included with the product. For details on the target interface, see the next chapter.

Note

To use PALMiCE3, the interface connector for PALMiCE3 use needs to be mounted on the target system beforehand.



PALMiCE3 JTAG200 model
Connection structure

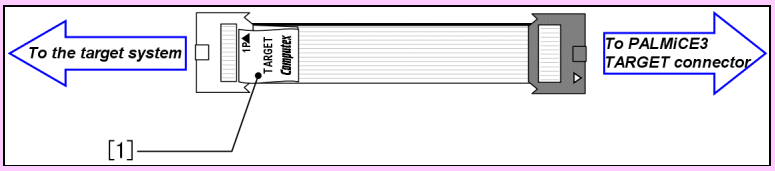
Note

When connecting the hardware,
if you put too much pressure, stress, or strain on the connector, doing so may cause damage.
Be careful not to put too much pressure or try not to strain or put stress on the connector.

Note

About target cable specifically for PALMiCE3

- Make sure to use PALMiCE3-specific target cable made by Computex.
- When establishing connections, connect the connector with a tag ([1] in the illustration) to the target system.



Info.

For connection to the target system, optional products such as conversion adapter are available.

Chapter 2
PALMiCE3 JTAG200 Hardware Specifications

2.1 PALMiCE3 JTAG200 model hardware specifications

PALMiCE3 is a purpose-built debugger for utilizing on-chip debugging feature incorporated in ARM-made cores.

PALMiCE3 incorporates on-chip debugging feature to provide the following functionalities.

- Execution and break of the user program
- Break by matching any address and data
- Force break of the user program
- Trace and step executions
- Viewing and editing of memory, register, and I/O

This chapter spells out specifications of PALMiCE3 hardware.

2.2 JTAG200 model specifications

Item		JTAG200 model specifications
Target interface		JTAG, SWD/SWV
Interface on the main unit side	Specification of the connector	20-pin MIL connector (Cable length: Approx. 20cm)
	Specification of the connector on the target system side	OMRON-made XG4C2031 (20-lead)
Target interface voltage		1.0V - 5.5V*1 (Follows target)
LED		・PWR ・BSY ・STS
Outside dimensions		95mm(W)X70mm(D)X21mm(H) (Exclusive of connector)
Operating environment		Operating temperature：5℃ to 40℃ Operating humidity： 35% to 85%RH No condensation
USB host interface		USB(Ver2.0)
AC adapter		Not required (Vbus support)
Current consumption		DC5V ±5% Max. approx. 250mA (from USB VBus)
Weight		78g

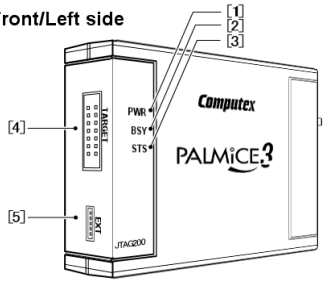
Note

*1 : Hardware revision "0-0" supports 1.0V - 3.6V.
For hardware revision, see "**2.3.1 Hardware revision**"

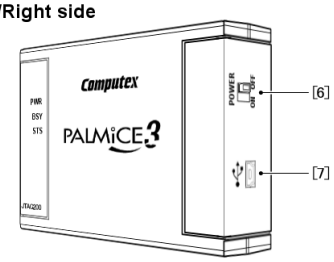
2.3 Name and function of each part

Appearance drawing of PALMiCE3 JTAG200 model is given to the following.

Front/Left side



Front/Right side



[1] PWR LED
Comes on when the power is supplied to PALMiCE3. Power is supplied from the host computer through USB cable.

[2] BSY LED
Flickers during communication between PALMiCE3 and the target CPU.

[3] STS LED
Lit normally during user program execution.
Also, flashes in some cases to notify errors.
For details, refer to the user's manual.

[4] TARGET connector
20-pin connector for connecting PALMiCE3 to the target system.

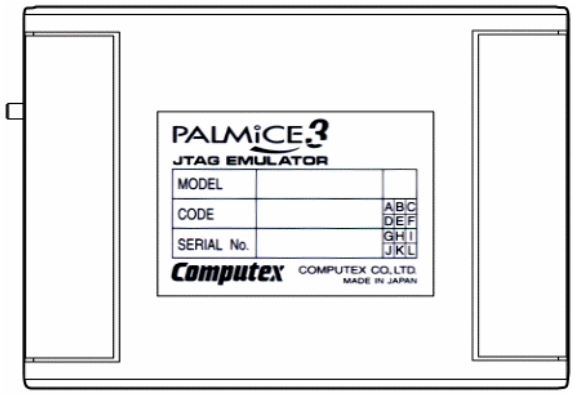
[5] EXT
Connect an optional cable. It is normally not used.

[6] Power switch
Turns ON/OFF the PALMiCE3's power. Power input state can be checked with [1] POWER LED.

[7] USB connector
Connect USB cable (mini-B type).

2.3.1 Hardware revision

The sticker with PALMiCE3 information is placed at the back of PALMiCE3 main unit.



Back side of PALMiCE3 main unit

How revision sticker reads

Read the number given on the upper side and the last alphabet shaded with black.

Example 1): Hardware revision 1-B

1		
A	**B**	C
D	E	F
G	H	I
J	K	L

In Example 1), PALMiCE3 hardware revision reads as 1-B.

Example 2): Hardware revision 2-0

2		
A	B	C
D	E	F
G	H	I
J	K	L

In Example 2), where alphabets are not shaded, PALMiCE3 hardware revision reads as 2-0.

Chapter 3 Target Interface Specifications

3.1 Introduction

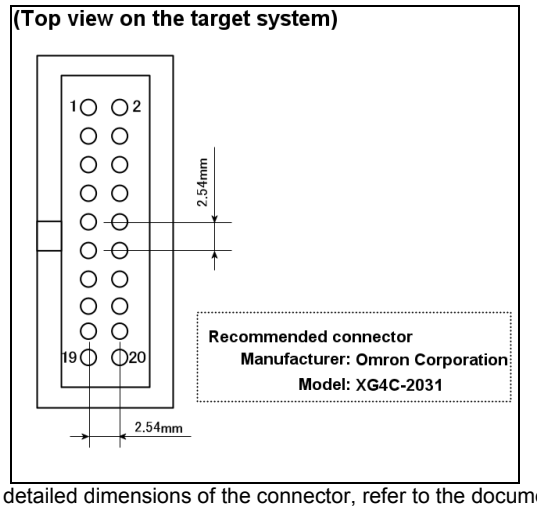
This Chapter spells out target interface specifications for connecting PALMiCE3 JTAG200 to the target system.

3.2 Target interface

The interface for connecting PALMiCE3 JTAG200 to the target system is described.
Target interface varies from CPU to CPU.

3.2.1 Shape of the connector for debugger

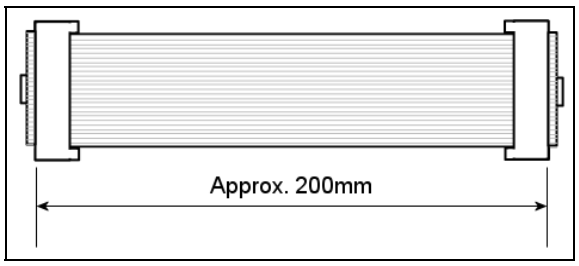
The shape of connector (20-pin MIL connector) for debugger to be mounted on the target system side is as follows.



(For detailed dimensions of the connector, refer to the documentations provided by manufacturers.)

3.2.2 Dimension of the target cable

The dimension of target cable for connecting PALMiCE3 JTAG200 to the target system is as follows.



(For detailed dimensions of the connector, refer to the documentations provided by manufacturers.)

3.2.3 Specifications of target interface signals

Input voltage level	VIL	Target voltage ÷ 2 – 0.35
	VIH	Target voltage ÷ 2 + 0.35
Output voltage level	VOL	Under 0.2V

3.2.4 The target interface on PALMiCE3 side

The target interface on PALMiCE3 side is described.

No.	Signal	Input/Output	Remarks	No.	Signal	Input/Output	Remarks
1	VTref*1	Output	550KΩ Pull-down	2	TVDD	Output	Not used
3	$\overline{\text{TRST}}$	Input	100Ω Series	4	GND		
5	TDI(N.C.*4)	Input	33Ω Series 10KΩ Pull-up*2	6	GND		
7	TMS(SWDIO*4)	Input (Input/Output*4)	33Ω Series 10KΩ Pull-up*2	8	GND		
9	TCK(SWCLK*4)	Input	33Ω Series	10	GND		
11	RTCK(N.C.*4)	Output	33Ω Series 100KΩ Pull-down	12	GND		
13	TDO(SWO*4)	Output	33Ω Series 10KΩ Pull-up*2	14	GND		
15	$\overline{\text{SRST}}$*3	Input	100Ω Series Open-collector	16	GND		
17	DBGRQ(N.C.*4)	Input	33Ω Series	18	GND		
19	DBGACK(N.C.*4)	Output	33Ω Series 100KΩ Pull-down	20	GND		

*1 : For VTref pin, connect the signal to the power at the same voltage level as the target interface. VTref pin is to serve for potential detection, and pull-up signal of 1KΩ will do.
*2 : Each of these signals has been pulled up to the voltage level detected from VTref pin.
*3 : It is an output signal with open-collector specification from PALMiCE3. Pull it up at a few KΩ (10KΩ recommended) on the target side.
*4 : Names of signals in ( ) are those for the time of Serial Wire Debugging. N.C. indicates that the pin is not used.

Note

Each name of the signal varies depending on the CPU you use.

Note

For Target connection reference diagram, refer to "PALMiCE3 Technical Information" up on Computex website (http://www.computex.co.jp/eg/)

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PALMiCE3 JTAG200 model Hardware Manual
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Our Tokyo Sales Office has been relocated to the following address since October 2013.

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